CLAIMS

What is claimed is:

1. A semiconductor memory device comprising:

a delay locked loop; and

a control signal generator that generates a first control signal and a second control signal, which are responsive to a plurality of mode selection signals for selecting operation modes of the semiconductor memory device, the first and second control signals to partially turn the delay locked loop on or off.

2. The semiconductor memory device of claim 1, wherein if the first control signal or the second control signal is activated, a portion of the delay locked loop to which the first or second control signal is applied is turned off.

3. The semiconductor memory device of claim 1, wherein if the first control signal or the second control signal is deactivated, a portion of the delay locked loop to which the first or second control signal is applied is turned on.

4. The semiconductor memory device of claim 1, wherein if a first of the plurality of mode selection signals is activated, only the second control signal is activated.

5. The semiconductor memory device of claim 1, wherein if a second of the plurality of mode selection signals is activated, the first and second control signals are deactivated.

6. The semiconductor memory device of claim 1, wherein if at least one of a third through fifth of the plurality of mode selection signals is activated, the first and second control signals are activated.

7. The semiconductor memory device of claim 1, wherein the control signal generator includes;

a first NOR gate for performing a NOR operation on a third through fifth of the plurality of mode selection signals;

a second NOR gate for performing a NOR operation on a third and fourth of the plurality of mode selection signals;

a third NOR gate for performing a NOR operation on a fifth and first of the plurality of mode selection signals;

a fourth NOR gate for performing a NOR operation on outputs of the second and third NOR gates;

a fifth NOR gate for performing a NOR operation on an output of the first NOR gate and a second of the plurality of mode selection signals to output the first control signal; and

a sixth NOR gate for performing a NOR operation on an output of the fourth NOR gate and a second of the plurality of mode selection signals to output the second control signal.

8. The semiconductor memory device of claim 1, wherein if a first of the plurality of mode selection signals is activated, the semiconductor memory device is in an active-power-down mode, if a second of the plurality of mode selection signals is activated, the semiconductor memory device is in an active-standby mode, if a third of the plurality of mode selection signals is activated, the semiconductor memory device is in a precharge mode, if a fourth of the plurality of mode selection signals is activated, the semiconductor memory device is in a precharge-power-down mode, and if a fifth of the plurality of mode selection signals is activated, the semiconductor memory device is in a self-refresh mode.

9. A semiconductor memory device comprising:

a delay locked loop;

a mode selection signal generator that generates a plurality of mode selection signals, which are responsive to operation control signals for controlling operations of

the semiconductor memory device, to select operation modes of the semiconductor memory device; and

a control signal generator that generates a first control signal and a second control signal, which are responsive to the plurality of mode selection signals, to partially turn the delay locked loop on or off.

10. The semiconductor memory device of claim 9, wherein if at least one of a third through fifth of the plurality of mode selection signals is activated, both the first and second control signals are activated.

11. The semiconductor memory device of claim 9, wherein if a first of the plurality of mode selection signals is activated, only the second control signal is activated.

12. The semiconductor memory device of claim 9, wherein if a second of the plurality of mode selection signals is activated, both the first and second control signals are deactivated.

13. The semiconductor memory device of claim 9, wherein the delay locked loop includes:

an input buffer that receives an external clock signal;

first and second delay units that compare a phase of a signal output from the input buffer with a phase of a predetermined internal clock signal, and delay the output signal of the input buffer in response to the comparison result, the first and second delay units being serially connected with each other;

an output unit that receives a signal output from the second delay unit, and outputs the received signal; and

a compensation feedback unit that delays the output signal of the second delay unit for the same time as the output signal of the second delay unit is delayed by the output unit, and outputs the delayed signal as the internal clock signal.

14. The semiconductor memory device of claim 13, wherein if the first control signal and the second control signal are activated, the input buffer, the first and second delay units, the output unit, and the compensation feedback unit are all turned off.

15. The semiconductor memory device of claim 13, wherein if the first control signal and the second control signal are deactivated, the input buffer, the first and second delay units, the output unit, and the compensation feedback unit are all turned on.

16. The semiconductor memory device of claim 13, wherein if only the second control signal is activated, the second delay unit, the output unit and the compensation feedback unit are turned off and the input buffer and the first delay unit are all turned on.

17. The semiconductor memory device of claim 13, wherein if only the second control signal is activated, the first delay unit, the second delay unit, the compensation feedback unit, and the output unit are turned off and the input buffer is turned on.

18. The semiconductor memory device of claim 9, wherein the control signal generator includes:

a first NOR gate for performing a NOR operation on a third through fifth of the plurality of mode selection signals;

a second NOR gate for performing a NOR operation on third and fourth of the plurality of mode selection signals;

a third NOR gate for performing a NOR operation on fifth and first of the plurality of mode selection signals;

a fourth NOR gate for performing a NOR operation on outputs of the second and third NOR gates;

a fifth NOR gate for performing a NOR operation on an output of the first NOR gate and a second of the plurality of mode selection signals to output the first control signal; and

a sixth NOR gate for performing a NOR operation on an output of the fourth NOR gate and the second of the plurality of mode selection signals to output the second control signal.

19. The semiconductor memory device of claim 9, wherein if a first of the plurality of mode selection signals is activated, the semiconductor memory device is in an active-power-down mode, if a second of the plurality of mode selection signals is activated, the semiconductor memory device is in an active-standby mode, if a third of the plurality of mode selection signals is activated, the semiconductor memory device is in a precharge mode, if a fourth of the plurality of mode selection signals is activated, the semiconductor memory device is in a precharge-power-down mode, and if a fifth of the plurality of mode selection signals is activated, the semiconductor memory device is in a self-refresh mode.

20. The semiconductor memory device of claim 9, wherein the operation control signals include a /CS (chip select) signal, a /CAS (column address strobe) signal, a /RAS (row address strobe) signal, a /WE (write enable) signal, and a CKE (clock enable) signal.